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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,813	09/24/2003	Ramanand Venkata	ALT-282	7626

36981 7590 05/31/2006

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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,813	VENKATA ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16* is/are allowed.

6)☒ Claim(s) *1-7,10-13,17,19,22,24,25 and 27* is/are rejected.

7)☐ Claim(s) *8,9,14,15,18,20,21,23 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the communication filed on May 8, 2006.

2. Claims 1-27 are pending for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7, 10, 17, 19, 22, 24-25, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted of Prior Art (APA) in view of Gage et al., US 20040205432 ("Gage").

7. As per claim 1, APA discloses a serial interface for use in a programmable logic device, said serial interface comprising:

a plurality of channels, each of said channels including at least transmit circuitry;

a central control circuitry including at least one clock source for generating at least one transmit clock for used by the transmit circuitry in each of the channels, each the transmit clock having a respective first clock rate [paragraph 0002 – Spec.] However, APA does not teach clock division circuitry in at least one of the channels for providing from at least one transmit clock a channel-derived clock having a second clock rate at most equal to the respective first clock rate.

Gage teaches another multi-channel architecture [fig. 2] comprising a central master clock generator for generating a central master clock signal for used by the transmit circuitry in each of the channels[1]. Specifically, Gage teaches a clock division circuitry in a plurality of said channels [paragraph 0030] for providing from at least one said clock a channel derived having a second clock rate at most equal to the respective first clock rate, the clock division circuitry in each of the plurality of channels being controllable independently of the clock division circuitry in any other of the plurality of channel [paragraph 0014, 0031].

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of APA with each channel having a separate

[1] The device comprises a frequency based testhead wherein the testhead further includes a plurality of channel card, each of the channel cards including synthesizer circuitry for creating a local frequency based variable clock signal of a difference frequency than the first frequency [paragraph 0012, 000029].

clock division circuitry as taught by Gage in order to allow each channel the ability to varying the clock rate at each channel.

8. As per claim 2, Gage teaches each of the channels includes the clock division circuitry [paragraph 0030].

9. As per claim 3, Although not explicitly taught in Gage that the respective first divider selectably divides the respective first clock rate by one of a group of at least one integer value. However, because Gage does not explicitly prohibit the divider from selectively divide the first clock rate by one of integer value and because the division by an integer in the clock divider circuit is such a well know means to modify the clock rate, it would have been obvious by design choice to modify the clock rate of Gage system by using one of a group of at least one integer value.

10. As per claim 5, well know.

11. As per claim 6, obvious.

12. As per claim 7, obvious.

13. As per claim 10, Gage teaches the at least one clock source consists of a single clock source [paragraph 0023] generating a single transmit clock having a single transmit clock rate.

14. As per claim 17, Gage does not explicitly teach the programmable logic device comprising the serial interface, however, Gage teaches a device that capable of connecting to one or more individual DUT. Therefore, it is obvious to one of ordinary skill in the art that Gage's generic interface included the claimed serial interface since the special interface does not effect the fundamental function of Gage's system.

15. As per claim 19, APA.

16. As per claim 22, see discussion in claim 17.

17. As per claim 24, obvious.

18. As per claim 25, the system is well know in the art of computer architecture.

19. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted of Prior Art (APA) in view of Gage.

20. As per claim 27, APA teaches a programmable logic device comprising:

a programmable logic core; and

serial interface means comprising:

a plurality of channel means, each of the channel means including a least transmit means;

a central control circuitry including at least one clock source for generating at least one transmit clock for used by the transmit circuitry in each of the channels, each the transmit clock having a respective first clock rate [paragraph 0002 – Spec.] However, APA does not teach clock division circuitry in at least one of the channels for providing from at least one transmit

clock a channel-derived clock having a second clock rate at most equal to the respective first clock rate.

Gage teaches Gage teaches another multi-channel architecture [fig. 2] comprising a central master clock generator for generating a central master clock signal for used by the transmit circuitry in each of the channels [see further discussion in claim 1].

21. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gage as applied to claim 1 above, and further in view of Swoboda et al. U.S. 5,903,746.

22. As per claim 11, Gage only teach one clock source. However, Swoboda et al. teach another clock acquisition subsystem for a data processing system has an interlocked clock multiplexer for acquiring a clock source which is provided as clock signal to the data processing system. Specifically, Swoboda et al teach the at least one clock source comprises a plurality of clock sources, each of the clock sources generating its own respective first clock rate [col. 2 lines 6-11; col. 3 lines 9-20].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Gage with the multiple clock sources as taught by Swoboda et al. in order to optimized the operation of the system [col. 3 lines 26-32].

23. As per claim 12, Swoboda et al. teach a selector for selecting one of the plurality of clock sources [col. 3 lines 29-38] and

it would have been obvious to one of ordinary skill that the combine teachings of Gage and Swoboda et al. teach the selecting of the plurality of clock sources and output of the clock division circuitry.

24. As per claim 13, Swoboda et al. teach the selector comprises a multiplexer [100 fig. 1].

Allowable Subject Matter

25. Claim 16 allowed.

26. Claims 8-9, 14-15 18, 20-21, 23, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

27. Applicant's arguments filed May 8, 2006, with respect to Final Action have been fully considered and are persuasive. The Final Action of 3/15/06 has been withdrawn.

28. Applicant's arguments with respect to claim 1-7, 10-13, 17, 19, 22, 24, 25 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran.